



## 3205, 3404

### 3205 HIGH SPEED 1 OUT OF 8 BINARY DECODER

### 3404 HIGH SPEED 6-BIT LATCH

- 18ns Max. Delay Over 0°C to 75°C Temperature: 3205
- 12ns Max. Data to Output Delay Over 0°C to 75°C Temperature: 3404
- Directly Compatible With DTL and TTL Logic Circuits
- Totem-Pole Output
- Low Input Load Current: .25mA Max., 1/6 Standard TTL input Load
- Minimum Line Reflection: Low Voltage Diode Input Clamp
- Outputs Sink 10mA Min.
- 16-Pin Dual In-Line Package
- Simple Expansion: Enable Inputs

#### 3205

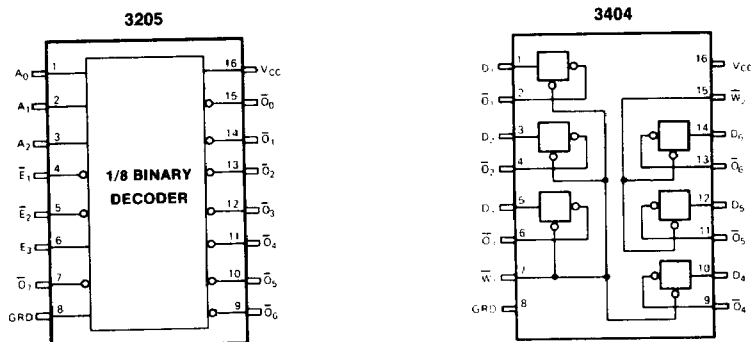
The 3205 decoder can be used for expansion of systems which utilize memory components with active low chip select input. When the 3205 is enabled, one of its eight outputs goes "low", thus a single row of a memory system is selected. The 3 chip enable inputs on the 3205 allow easy memory expansion. For very large memory systems, 3205 decoders can be cascaded such that each decoder can drive 8 other decoders for arbitrary memory expansions.

#### 3404

The Intel 3404 contains six high speed latches organized as independent 4-bit and 2-bit latches. They are designed for use as memory data registers, address registers, or other storage elements. The latches act as high speed inverters when the "Write" input is "low".

The Intel 3404 is packaged in a standard 16-pin dual-in-line package; and its performance is specified over the temperature range of 0°C to +75°C, ambient. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffusion process.

#### PIN CONFIGURATION



**ABSOLUTE MAXIMUM RATINGS\***

Temperature Under Bias:	Ceramic	-65°C to +125°C
	Plastic	-65°C to +75°C
Storage Temperature		-65°C to +160°C
All Output or Supply Voltages		-0.5 to +7 Volts
All Input Voltages		-1.0 to +5.5 Volts
Output Currents		125 mA

**\*COMMENT**

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. CHARACTERISTICS**  $T_A = 0^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

**3205, 3404**

SYMBOL	PARAMETER	LIMIT		UNIT	TEST CONDITIONS
		MIN.	MAX.		
$I_F$	INPUT LOAD CURRENT		-0.25	mA	$V_{CC} = 5.25\text{V}$ , $V_F = 0.45\text{V}$
$I_R$	INPUT LEAKAGE CURRENT		10	$\mu\text{A}$	$V_{CC} = 5.25\text{V}$ , $V_R = 5.25\text{V}$
$V_C$	INPUT FORWARD CLAMP VOLTAGE		-1.0	V	$V_{CC} = 4.75\text{V}$ , $I_C = -5.0\text{mA}$
$V_{OL}$	OUTPUT "LOW" VOLTAGE		0.45	V	$V_{CC} = 4.75\text{V}$ , $I_{OL} = 10.0\text{mA}$
$V_{OH}$	OUTPUT HIGH VOLTAGE	2.4		V	$V_{CC} = 4.75\text{V}$ , $I_{OH} = -1.5\text{mA}$
$V_{IL}$	INPUT "LOW" VOLTAGE		0.85	V	$V_{CC} = 5.0\text{V}$
$V_{IH}$	INPUT "HIGH" VOLTAGE	2.0		V	$V_{CC} = 5.0\text{V}$
$I_{SC}$	OUTPUT HIGH SHORT CIRCUIT CURRENT	-40	-120	mA	$V_{CC} = 5.0\text{V}$ , $V_{OUT} = 0\text{V}$
$V_{OX}$	OUTPUT "LOW" VOLTAGE @ HIGH CURRENT		0.8	V	$V_{CC} = 5.0\text{V}$ , $I_{OX} = 40\text{mA}$

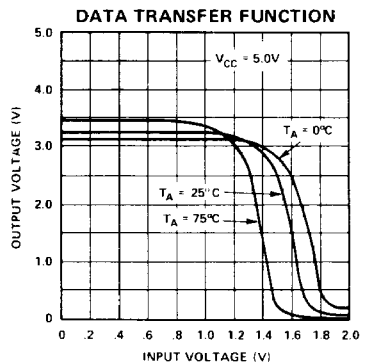
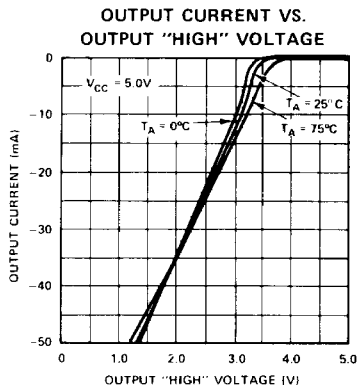
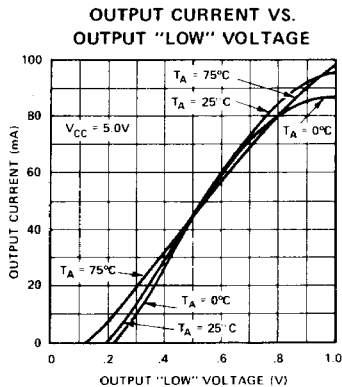
**3205 ONLY**

$I_{CC}$	POWER SUPPLY CURRENT		70	mA	$V_{CC} = 5.25\text{V}$ , Outputs Open
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**3404 ONLY**

$I_{CC}$	POWER SUPPLY CURRENT		75	mA	$V_{CC} = 5.25\text{V}$ , Outputs Open
$I_{FW1}$	WRITE ENABLE LOAD CURRENT PIN 7		-1.00	mA	$V_{CC} = 5.25\text{V}$ , $V_W = 0.45\text{V}$
$I_{FW2}$	WRITE ENABLE LOAD CURRENT PIN 15		-0.50	mA	$V_{CC} = 5.25\text{V}$ , $V_W = 0.45\text{V}$
$I_{RW}$	WRITE ENABLE LEAKAGE CURRENT		10	$\mu\text{A}$	$V_R = 5.25\text{V}$

**TYPICAL CHARACTERISTICS**



# 3205 HIGH SPEED 1 OUT OF 8 BINARY DECODER

## SWITCHING CHARACTERISTICS

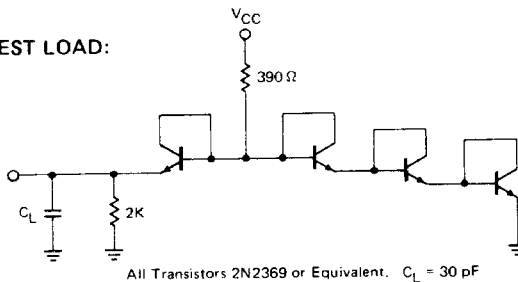
### CONDITIONS OF TEST:

Input pulse amplitudes: 2.5V

Input rise and fall times: 5 nsec  
between 1V and 2V

Measurements are made at 1.5V

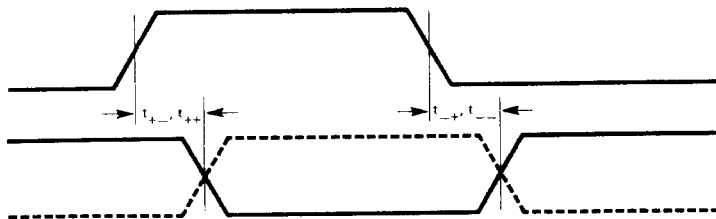
### TEST LOAD:



### TEST WAVEFORMS

ADDRESS OR ENABLE  
INPUT PULSE

OUTPUT



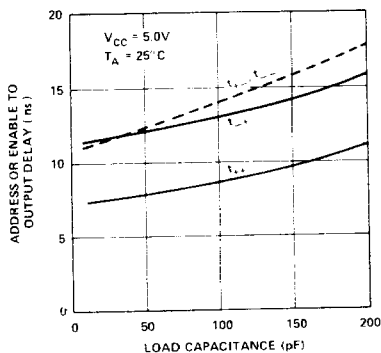
### A.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $+75^\circ\text{C}$ , $V_{CC} = 5.0\text{V} \pm 5\%$ unless otherwise specified.

SYMBOL	PARAMETER	MAX. LIMIT	UNIT	TEST CONDITIONS
$t_{+}$	ADDRESS OR ENABLE TO OUTPUT DELAY	18	ns	
$t_{-+}$		18	ns	
$t_{+-}$		18	ns	
$t_{-}$		18	ns	
$C_{IN}^{(1)}$	INPUT CAPACITANCE	4(typ.) 5(typ.)	pF pF	$f = 1\text{ MHz}$ , $V_{CC} = 0\text{V}$ $V_{BIAS} = 2.0\text{V}$ , $T_A = 25^\circ\text{C}$

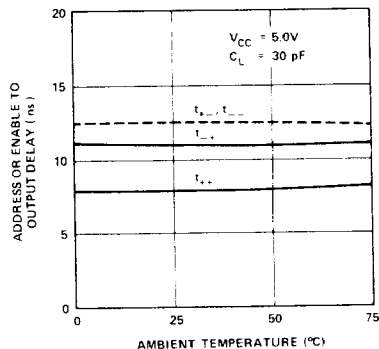
1. This parameter is periodically sampled and is not 100% tested.

### TYPICAL CHARACTERISTICS

ADDRESS OR ENABLE TO OUTPUT  
DELAY VS. LOAD CAPACITANCE



ADDRESS OR ENABLE TO OUTPUT  
DELAY VS. AMBIENT TEMPERATURE



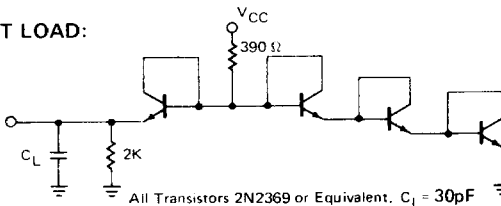
# 3404 6-BIT LATCH

## SWITCHING CHARACTERISTICS

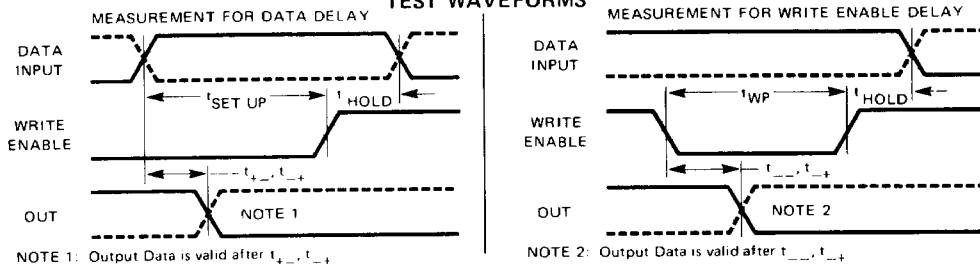
### CONDITIONS OF TEST:

Input pulse amplitudes: 2.5V  
 Input rise and fall times: 5 nsec between 1V and 2V  
 Measurements are made at 1.5V

### TEST LOAD:



### TEST WAVEFORMS

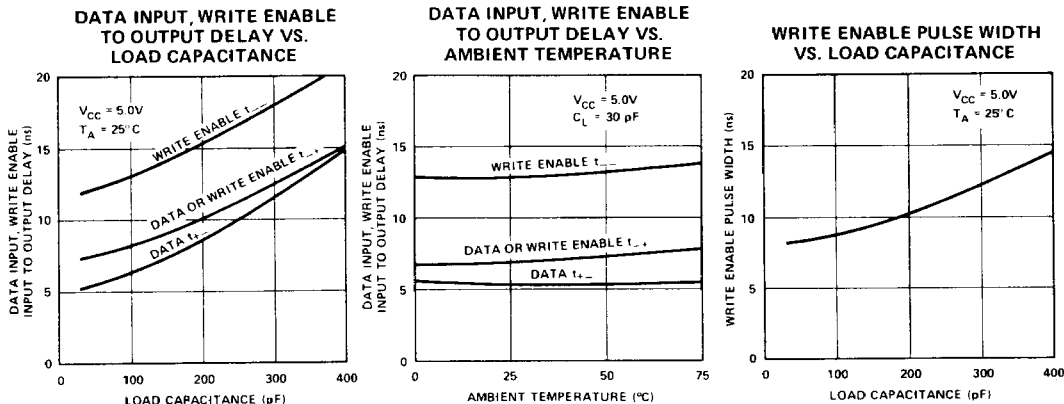


## A.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $+75^\circ\text{C}$ , $V_{CC} = 5.0\text{V} \pm 5\%$ ; unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
$t_{+ \dots t_{-+}}$	DATA TO OUTPUT DELAY			12	ns	
$t_{- \dots t_{-+}}$	WRITE ENABLE TO OUTPUT DELAY			17	ns	
$t_{\text{SET UP}}$	TIME DATA MUST BE PRESENT BEFORE RISING EDGE OF WRITE ENABLE	12			ns	
$t_{\text{HOLD}}$	TIME DATA MUST REMAIN AFTER RISING EDGE OF WRITE ENABLE	8			ns	
$t_{\text{WP}}$	WRITE ENABLE PULSE WIDTH	15			ns	
$C_{\text{IND}}^{(3)}$	DATA INPUT CAPACITANCE	P3404	4		$\mu\text{F}$	$f = 1 \text{ MHz}, V_{CC} = 0\text{V}$
		C3404	5		$\mu\text{F}$	$V_{\text{BIAS}} = 2.0\text{V}, T_A = 25^\circ\text{C}$
$C_{\text{INW}}^{(3)}$	WRITE ENABLE CAPACITANCE	P3404	7		$\mu\text{F}$	$f = 1 \text{ MHz}, V_{CC} = 0\text{V}$
		C3404	8		$\mu\text{F}$	$V_{\text{BIAS}} = 2.0\text{V}, T_A = 25^\circ\text{C}$

NOTE 3: This parameter is periodically sampled and is not 100% tested.

## TYPICAL CHARACTERISTICS



ROM/PROM